# Measuring Material, Dopant Loss

## From Post-Implant Wafer Cleans

Maintaining the integrity of ultrashallow junctions (USJs) after exposure to an increasing number of high-dose implant resist cleaning steps is critical for logic device manufacturing at the 45 nm node and beyond. Use of SiGe in the PMOS regions adds an additional material challenge. A new short loop method provides accurate relative measurements of amorphized silicon or SiGe loss caused by different types of strip/clean processes.

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The International Technology Roadmap for Semiconductors (ITRS) estimates silicon loss requirements for logic devices to be <0.3 Å per cleaning step for the 45 nm technology node, and 0.2 Å per clean for 32 nm.[1] The allowable loss for the 10 or more front-end-of-line (FEOL) cleaning steps for heavily implanted photoresist, as well as other cleans, is roughly 3 Å total. The acceptable SiGe loss for raised source/drain (S/D) is not as well defined, but the effect of cleaning processes on SiGe will become more critical as its integration moves into the channel.

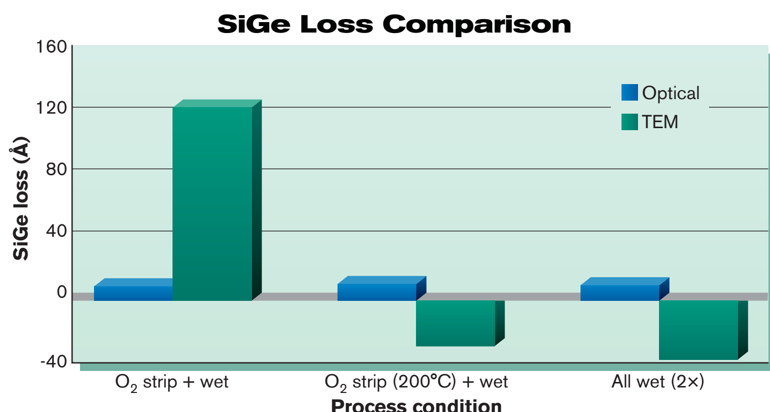
Clearly, controlling the effects of the cleaning processes on the SiGe is necessary for device properties to be optimized. In the future, these same concerns will also affect the manufacture of memory devices as they adopt advanced materials and techniques to enable continued geometry shrinks. In fact, epitaxial silicon is already being used for building elevated S/Ds to improve junction leakage and memory retention times in advanced DRAM devices.[2]

Optimization of the strip/clean processes is essential for both yield and device characteristics. Perhaps the most critical FEOL cleaning steps are after high-dose ion implant (HDIS). As devices shrink, it is increasingly difficult to maintain cleaning efficiency for post-ash residues while meeting increasingly stringent damage/oxidation/loss specifications of the ultrashallow junctions (USJs) or other critical materials.[1] Such residues, if left behind, would cause high contact resistances or affect device reliability. However, an overly aggressive cleaning approach would lead to material/dopant loss, changing the electrical characteristics of the device by increasing sheet resistance ($R_s$) and reducing S/D drive current.[3,4]

Many manufacturers are trying various approaches to reducing silicon and SiGe loss. Some are reducing SC1 wet clean temperature, but this also reduces the effectiveness of the residue and particle removal, putting more burden on the dry strip process. Likewise, for some lower-energy and/or lower-dose implant levels, plasma strip with non-oxidizing chemistries have been found to reduce silicon oxidation, but could reduce cleaning efficiency, depending on implant conditions.

For logic devices that use SiGe for strain engineering, matters are complicated by the need to determine the effect of the cleaning processes where epitaxial SiGe is exposed. Because of solubility of $GeO_2$ in water, SiGe loss may be very different from the silicon loss. Furthermore, the loss for doped (amorphized) SiGe may be very different from the loss for crystalline SiGe, where accurate and inexpensive optical measurements are easily made.

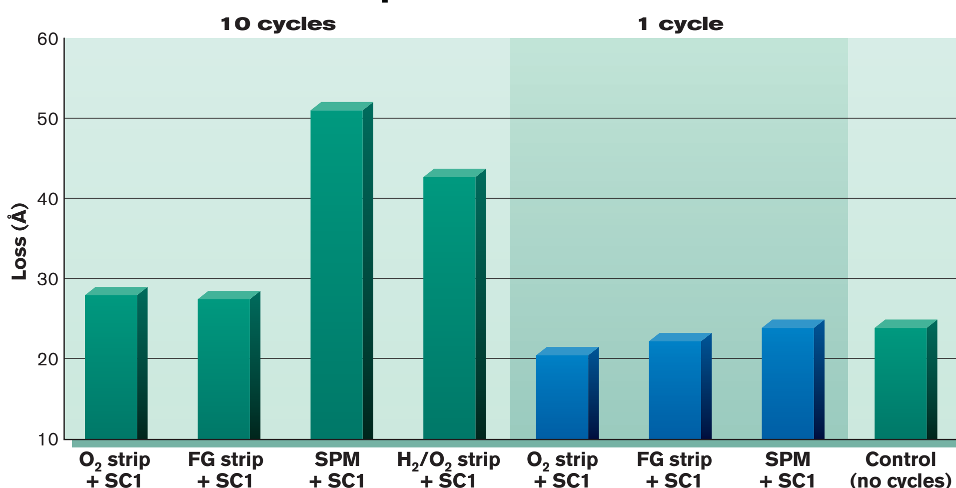
The TEM approach is currently the default method for measuring junction material losses, but has several drawbacks. Wafers are typically processed on short or full process flows that are both timely and expensive. The TEM measurement process itself is slow, and manual involvement needed for the sample preparation can introduce error. Since it is practical to limit the number of measurements, and often without control, this error can go unrecognized. In fact, an attempt was made to use TEMs for this study, but the




**1. Researchers used both optical and TEM methods to measure SiGe loss for various dry strip/wet clean processes. Variations in the TEM measurements, however, were too extreme and not credible.**

variations were too extreme and not credible (Fig. 1).

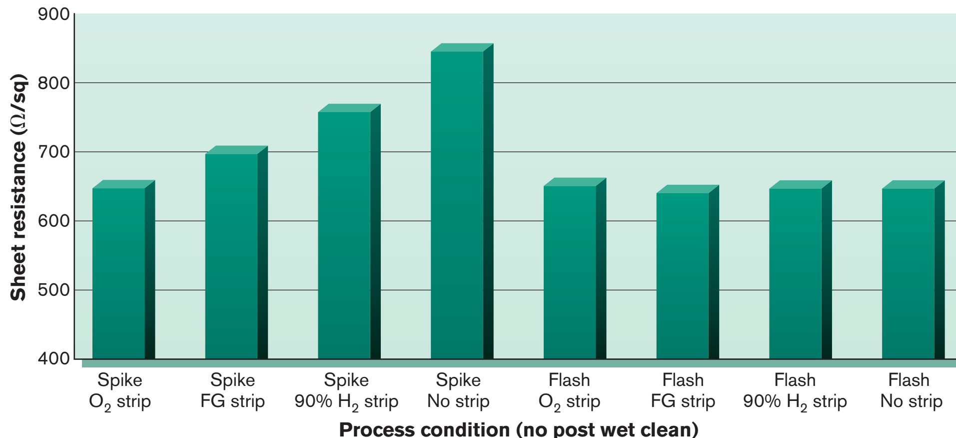
This clearly shows the need for a measurement method allowing quick, accurate and low-cost monitoring of junction recess effects of dry strip and wet cleaning processes. A fast, non-destructive optical approach would be ideal. But because optical properties of heavily implanted (doped) silicon or SiGe vary with temperature history, and are unstable, accurate measurements of the thickness is very difficult. The method described in this paper allows the use of optical measurement methods using blanket amorphized silicon or SiGe wafers in a process sequence that reflects actual product process flows.




**2.** This chart compares amorphous silicon loss for different strip/clean chemistries, along with a variation in the number of cycles. A passivating effect of the grown oxide is seen in the fact that the wafers with 10 strip/clean cycles have far less than 10× the silicon losses of the single-cycle wafers.

## Experimental procedure

The first step in this method for measuring doped SiGe loss involves reproducing the α-SiGe material after exposure to the effects of implant, dry strip and wet clean processes. This requires implants of xenon or arsenic ions into unpatterned, blanket SiGe films on bulk silicon wafers.




**3.** Measurements show the effect on sheet resistance of ion implanted silicon (2 keV, $10^{15}$ $As^+$) using various strip/clean processes and different annealing thermal budgets. For the flash anneal, the final sheet rho was clearly independent of the strip/clean type, indicating there was very little out-diffusion during the anneal.

Steps to measure SiGe loss:

1. A layer of SiGe was grown at the desired thickness and composition on bulk silicon wafers. The SiGe material at junctions used for S/D stress engineering is typically ~20% germanium content and 60-70 nm thickness.

2. Next, SiGe film thickness was measured with an ellipsometer-based thin-film measurement tool, an F5X from KLA-Tencor (the measured stack was SiGe/Si with a typical goodness of fit (GOF)≥0.95).

3. SiGe films (with no photoresist on them) were then implanted with either xenon (for material loss measurements) or arsenic (for dopant loss measurements). Both implants were done at an energy of ≤20 keV to produce an amorphized, surface layer calculated to be about half the thickness of the SiGe (verified by TRIM code[5] simulations prior to the implants). The implants leave an underlying layer of SiGe that remains crystalline and will later be used to regrow the crystal.

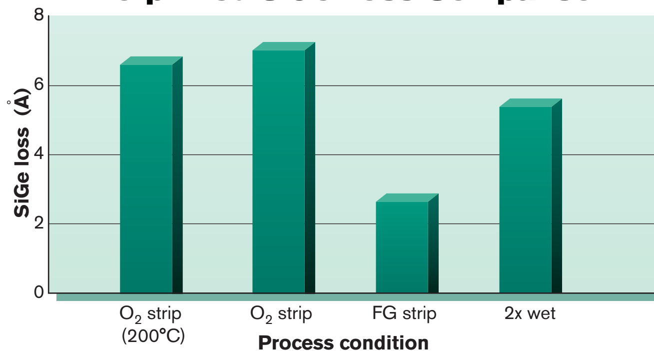
4. The wafers were then exposed to the various cleaning processes, including a few dry strip chemistries performed in a Mattson ICPHT source. All dry strip tests were done at 250°C unless otherwise noted, and were followed by wet cleans. One wafer was treated with an all-wet clean approach. Dry strips were done with gas mixtures that were either predominantly oxygen or oxygen-free. Wet cleans were standard SPM/SC1 combinations, where the SC1 temperature was typically 40°C, somewhat lower than the norm for 65 nm process flows. One control wafer was exposed to no strip or clean process. The control received only the appropriate implant, along with all the other test wafers, and was stored for the duration of the strip/clean processing until the anneal step described next.

5. Following the various cleans, the wafers (including the control) were promptly annealed with an appropriate rapid thermal (~1000°C spike anneal) process for the SiGe material. The conditions of the anneal were identical to what was used for 45 nm production wafers.

6. Once SiGe layers were annealed and the crystal regrown to the surface, the wafers were again measured by the ellipsometric film thickness tool. SiGe layer thicknesses were subtracted from their initially measured thicknesses to determine the amount of material that was oxidized or lost. The measured SiGe losses were then compared with that of the control wafer for the different cleaning conditions.

For determining dopant losses, sheet resistance was measured for arsenic-implanted wafers after anneal, including a control wafer that was not exposed to strip or clean processes. Resistivity measurements of silicon were performed using a non-contact sheet resistance me-

trology tool made by Frontier Semiconductor Measurement Inc. For the SiGe resistivity measurement, a Tencor RS100 four-point probe was used. Results of sheet resistance measurements for the various strip/clean conditions show the relative effects on the activated dopant in the SiGe after anneal.




**4.** This chart compares the amorphized SiGe loss for various dry strip processes and wet cleans. The dry process was performed four times with a standard SPM/SC1 after each dry strip. (Note: normalized data - control wafer = no loss; GOF≥0.95)

### Silicon characterization

This method was initially evaluated for measuring α-Si loss on silicon-on-insulator (SOI) wafers (Fig. 2). In the case of the control wafer, 25 Å of silicon was consumed during the implant, queue time and anneal. This can be explained by the sputtering caused by the ion implant and the subsequent growth of native oxide during the excessive queue time between implant and the thickness measurement (about two weeks).

Clearly, the growth of native oxide was greater in the control than the sample that had been exposed to oxygen-based strip. This shows a passivating effect of the more densely grown oxide generated in the plasma environment, while native oxide apparently has less ability to prevent further silicon oxidation. Because of this, the control is not valid, and we must consider that all silicon losses shown in Figure 2 are relative.

This passivating effect of the grown oxide is seen in the fact that the wafers with 10 strip/clean cycles have far less than 10× the silicon losses of the single-cycle wafers. We believe that the ~5-7 Å of added silicon loss for 10 passes vs. one pass suggests that $O_2$ or forming gas (FG)-based strip/clean causes a total loss of ~1 Å per pass, consistent with reports from our customers. Interestingly, both oxygen and FG-based dry strip/wet clean wafers showed much less silicon loss than for the 10 passes of strong wet clean (SPM+SC1), which is used in many memory fabs.

The 10-pass $H_2$+$O_2$ wafer has much higher silicon loss than either oxygen or FG-based processed wafers, showing hydrogen's ability to assist in the oxidation, possibly due to a lowering of the activation energy for silicon oxidation. The non-oxygen, hydrogen-based stripped wafers show equivalent silicon loss to oxygen-based stripped wafers, demonstrating a similar passivating effect to oxygen-based, either due to nitridation of the surface or possibly surface activation allowing denser oxide growth during the wet cleans.

Measurements were also done showing the effect on sheet resistance of ion implanted silicon (2 keV, $10^{15}$ $As^+$) using various strip/clean processes and different annealing thermal budgets (Fig. 3). For the flash anneal, the final sheet resistance was clearly independent of the strip/clean type, indicating there was very little out-diffusion during the anneal. Further, there is little if any dependence of final sheet resistance on strip chemistry.

However, for a normal spike anneal, the sheet resistance was strongly affected by the presence of a passivating surface oxide. Here, the beneficial effect of the oxygen-based strip can be seen. The sheet resistance is highest for the control wafer, which was not exposed to strip or clean, and lowest for the wafer that had $O_2$-based strip. Clearly, the out-diffusion of dopant is less inhibited by the native oxide than it is by the more dense oxide grown under oxygen plasma conditions. There seems to be a higher density barrier for FG-based strip — almost equivalent to an oxygen-based strip — than for strip using gas mixtures with higher hydrogen content.

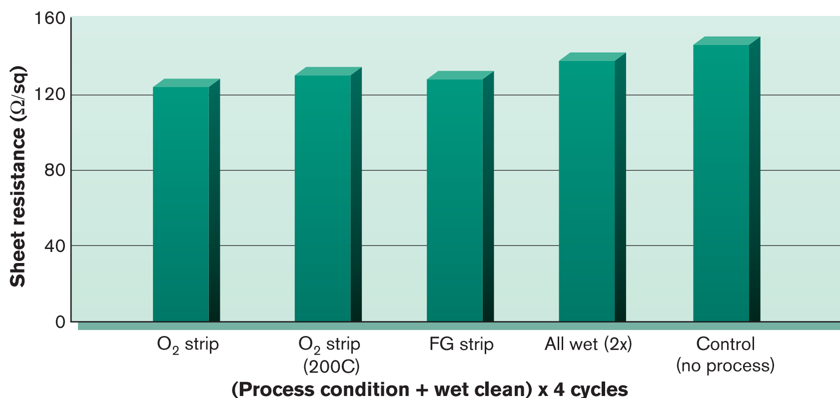
### SiGe characterization

Figure 4 shows the SiGe loss results for the same dry strip and wet clean processes used for the amorphous silicon testing. As in Figure 2, the dry process was performed four times with a standard SPM/SC1 after each dry strip. Queue time control was far superior to that for silicon loss tests shown previously, totaling about two days for the full process sequence.

The control wafer had very little or no SiGe loss with the xenon implant, despite the sputtering that must have taken place as well as native oxide growth. The fact that there is no SiGe loss at all in the control may be due to the metrology (measuring a SiGe/Si stack) — it is possible that the ellipsometer did not resolve the surface native oxide that must have grown, effectively increasing the SiGe thickness.

Figure 4 normalizes the data, setting the control as zero loss. The results show ~6 Å of SiGe loss for oxygen-based processes and wet cleans, but only ~3 Å with the FG-based strip. More oxidation/SiGe loss would be expected from the 250°C vs. the 200°C $O_2$ processes, but the temperature effect may have been offset by longer process times for the 200°C recipe. SiGe loss for all-wet strips was comparable to that for $O_2$-based strips, and about double that of the reducing chemistry strip with the same wet clean.

In dopant loss experiments with SiGe wa-




**5.** Blanket SiGe sheet resistance was measured for different strip conditions using spike anneal for a 20 keV $As^+$ implant.

fers, the queue time control was better than in the preceding silicon loss tests, and only standard spike RTP was used. It should be noted that each of the dry strip conditions included an SPM/SC1 wet clean. This combination cycled four times. The all-wet process of record (POR) is an SPM/SC1 clean repeated twice to achieve cleanliness equivalent to the dry/wet combination. This 2×-wet POR was also cycled four times in each POR, therefore giving eight wet clean cycles total.

The data shown (Fig. 5) indicates that the control wafer, as with silicon, has the highest sheet resistance — about 20% greater than that of the $O_2$-based strip. This means, as with silicon wafers, that the out-diffusion of dopant is greatest in this case, likely due to the native oxide permeability during anneal. Interestingly, it seems that the SPM/SC1 process, when repeated effectively eight times, results in less dopant loss than the eight total passes through the dry strip/wet clean combinations (four dry strip cycles + four wet clean cycles).

The fact that the $O_2$-based strip results in the lowest sheet resistance is also consistent with our results in silicon wafer tests. Relative to the 200°C strip, the $O_2$ strip at 250°C indicates that the grown oxide is a less permeable barrier to dopant diffusion.

The sheet resistance from the FG-based strip is only slightly higher than that from the $O_2$-based process at 250°C, and the same as that from the 200°C process. As in the case for silicon, this suggests that the FG process does have a passivating effect, either because of nitridation or because of a higher degree of oxidation being promoted in the wet processes.

## Conclusions

We have measured amorphous SiGe loss after exposure to multiple strip and clean processes with a new method initially used for measuring amorphous silicon loss with SOI wafers. This short-loop testing approach has been useful in measuring the relative material and dopant losses from both silicon and SiGe after high-dose implant.

This technique can be used to evaluate and optimize plasma/wet cleaning processes. In our study, material losses caused by dry strip/wet clean combinations were the same or less than that caused by an all-wet strip/clean approach. It is possible that this method could also be used as a simple, effective process control monitor. **SI**

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