

MEETING REQUIREMENTS FOR DRY STRIP OF HIGH-DOSE IMPLANTED RESIST AT THE 45 NM NODE

Stephen Savas, Stephen Hyatt, Vijay Vaniapura, Qin Ce, Bob Elliston, Chevan Goonetilleke, Hai-Au Phan-Vu
Mattson Technology, Inc.
47131 Bayside Parkway, Fremont, CA. 94538, USA
Stephen.Savas@Mattson.com

Abstract

The requirement for sub-ångström (Å) silicon (Si) and oxide loss during each post-implant stripping and cleaning step is among the most challenging in front-end-of-line (FEoL) integration at the 45 nanometer (nm) node and beyond. The main difficulty is in totally removing the very tough crosslinked carbon polymer and dopant crust remaining following high-dose ion implant while causing only sub-ångström loss, oxidation or damage to Si in junctions. We have recently developed a dry strip process in conjunction with standard soft wet cleans that achieves ≤ 1 Å (when associated with numbers, just use the symbol) total Si loss per strip and clean step. Si loss for the combined strip and cleaning processes has been measured with a novel technique that mimics actual process flows in integrated circuit (IC) production. We believe this method is more realistic and accurate than the conventional Si loss measurement techniques. Because the dry strip processes include steps containing hydrogen and no oxygen, we have done electrical, optical and chemical analysis of wafers following the doping/strip/anneal process flow. These tests show that the reducing strip processes cause less dopant loss, or damage, to silicon properties in ultra-shallow junctions (USJ) than oxygen-based strip processes.

Introduction

Resist stripping and wafer cleaning following high-dose ion implantation will increasingly impact device performance and yield at the 45 nm node and beyond. These effects stem respectively from loss of Si and dopant from junctions, and the increasing difficulty of full removal of defects in the cleaning steps following ion implant. Si and dopant loss, as well as pattern damage, constrain the chemical and physical intensity of the cleaning processes needed to remove both residues and particulates. Thus, device performance may be competing with the die yield in optimization of process flows. In this circumstance, the traditional dry stripping processes using oxygen as principal reactive feed gas, while having high rates of photoresist (PR) removal needed historically for stripping productivity, need to be re-examined for their impact on the optimization of the device performance and yield. Further, decreasing ion energies, particularly in the junction implants, as well as the use of thinner resist masks for all ion implants, mean that the very high stripping rates required in the past for acceptable stripping productivity are no longer needed.

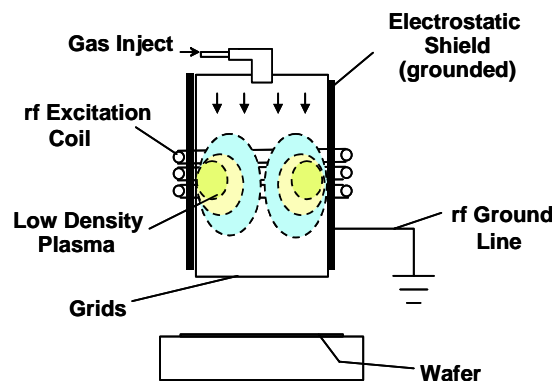
As a result of all these considerations, we have developed a stripping process using hydrogen as principal reactant for some, or all, of the dry stripping steps for removing high-dose

ion implanted PR. We have also generally avoided use of fluorinated gas, which is currently often used in facilitating residue removal. [1] These changes in process gas chemistry help achieve an optimized dry stripping and wet cleaning process. As with all new processes, it is essential to do accurate measurements of the effects on silicon and dopants from such chemistry changes. These measurements begin to provide validation of such new dry strip process chemistry for use in advanced device manufacturing. First, it is necessary to assure that combined dry strip and wafer clean processes remove resist and inorganic residues completely. Secondly, one must measure the Si loss due to such combined dry strip and wet clean steps, showing it meets device requirements for that technology generation. (Simply measuring Si loss due to the dry strip is not accurately reflective of the effect on devices since there is interaction between dry strip and wet clean processes, especially for strip processes using fluorine or ion bombardment.) Finally, one must verify that the properties of the silicon and the dopants following USJ anneal are not adversely affected by the novel chemistry of the dry stripping process. Such analyses have been completed for this new process chemistry and results are reported below.

System Description

We have used a downstream plasma-based stripping system (Suprema™) with an electrostatic shielded source. This system uses a grid between the plasma and the process region for ion filtering. A cross-section of the plasma source chamber is shown in Figure 1.

Figure 1. Schematic design of the inductively coupled plasma



(ICP) source used in processing wafers for this paper. The gases are injected at the top of the source, and the wafer process region is below the grids.

This source employs a grounded electrostatic shield for minimizing the sputtering and making wall conditions in the

source more uniform. Gas (typically several liters per minute total flow) is injected from the top of the source and flows down through the plasma and then through the grid into the wafer process region. Process pressure is generally maintained at the order of magnitude of 1 Torr. Plasma source power is provided by a radio frequency (rf) generator capable of 3 kW at 13.56 MHz. An automatch network assures that virtually all power provided to the match is usable. The wafer rests on a resistively heated temperature-controlled pedestal that provides a controllable and uniform process temperature.

Process Conditions and Results

We have tested reducing dry strip processes for a range of wafer conditions typical following USJ source/drain and extension implants. [2] Ion species included As⁺, P⁺ and B⁺ as well as BF₂⁺. Implanted ion energies ranged from about 3 keV to as much as 15 keV with doses from about 1 E15/cm² to about 4 E15/cm². Wafers with patterned photoresist (248 nm DUV PR), having thickness from approximately 3000 Å to 5000 Å and line/space widths ranging from approximately 150 nm to microns were used for this experiment. Typical dry strip process times ranged from about two minutes to as much as four minutes. Results on the wafer can be seen in SEM micrographs following dry strip only for varying amounts of oxygen in the feed gas.

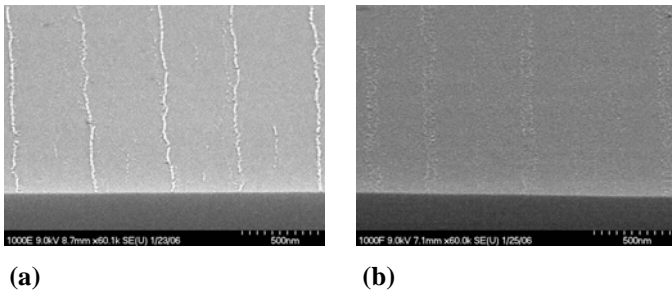
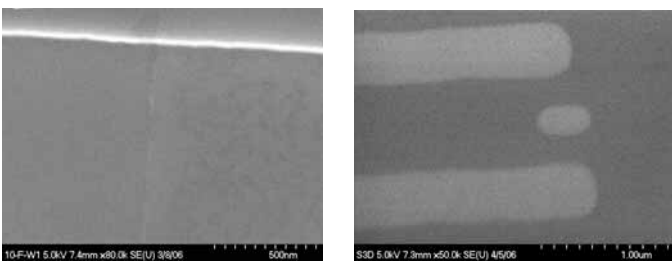


Figure 2. Residues, following dry strip only, of implanted (BF₂⁺ at 8 keV, 3 E15/cm²) DUV-patterned wafers for recipes having varying amounts of oxygen in one step. (a) 10% O₂ (b) No O₂

Recipes using no oxygen as seen in Figure 2(b) produce less substantial inorganic residue after dry strip alone. In Figure 3(a) and 3(b) are shown SEM micrographs of other implanted PR samples dry stripped using recipes based on the reducing chemistry, such as shown in Figure 2, and then wet cleaned. Such strips yield wafers whose residues are sufficiently degraded that a low-temperature SC1 with short wet cleaning times fully removes them. Extending process time of the dry strip process beyond that used for Figure 3 breaks down residues, permitting remaining residues to be removed by DI rinse alone. Results following DI rinse are shown in Figure 4(a) and 4(b). For both dopant types, and with implant energies and doses at least as large as those typically used for



source/drain or extension implants at the 45 nm node, the residues are removed.

(a) (b)

Figure 3. SEM micrographs show no remaining residues following combined dry strip recipes without O₂ in one or more steps following soft wet clean for implant conditions (a) P⁺ at >10 keV, > 3 E15/cm² (b) BF₂⁺ at > 4 keV, > 1 E15/cm².

This kind of process, using no exposure to wet chemistries that etch silicon dioxide or cause silicon oxidation, has the greatest potential for minimizing the Si loss at the junctions.

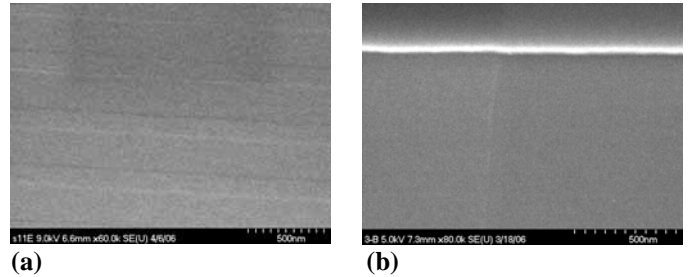


Figure 4. SEM micrographs of post-strip and DI Rinse for implanted DUV PR (~ 4000 Å) with line and space patterns. Implant conditions: (a) P⁺ at > 20 keV, > 2 E15/cm² (b) As⁺ at > 10 keV, > 3 E15/cm²

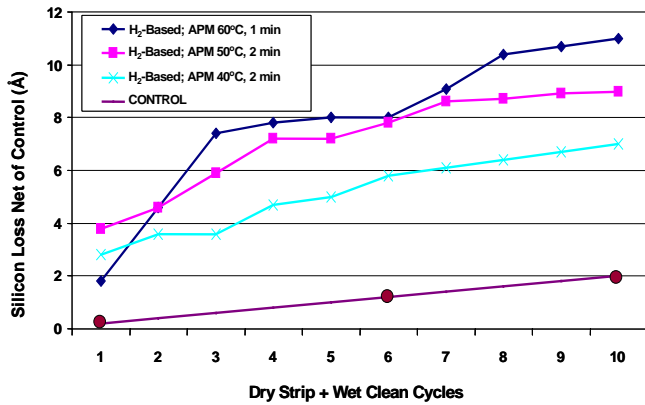
Having demonstrated complete residue removal, we turn to measurement of Si loss due to the combined dry strip and wet clean steps. It is most desirable to measure the combined loss of Si for the complete set of strip and wafer clean processes following the high-dose ion implants. In order to do this, we have developed a novel technique using silicon-on-insulator (SOI) wafers based on a method that was first suggested by a customer. This technique uses repeated exposures (up to 10) of SOI wafers to the sequence of alternating dry strip and wet clean with silicon layer thickness measured after each or every other wafer clean. This, somewhat mimics the process flow of device manufacturing, where the sequence of (PR patterning, ion implant, dry strip and wet clean) is repeated 12 times or more.

The results shown in Figure 5 are for dry strip and wet clean processes, of which the 40°C, two-minute recipe was used in producing results shown in SEMs of Figure 3. Notable is the fact that, for this recipe, the best Si loss is about 0.7 Å per strip and clean cycle with the process flow, including 10 high-dose implant (dry strip + wet clean) cycles.

Figure 5. Measured differences in Si layer thickness (minus control) for iterations of the (dry strip + wet clean) sequence for different (APM) temperatures and process times.

This combined strip and clean has been shown to yield clean wafer surfaces for most USJ implant conditions.

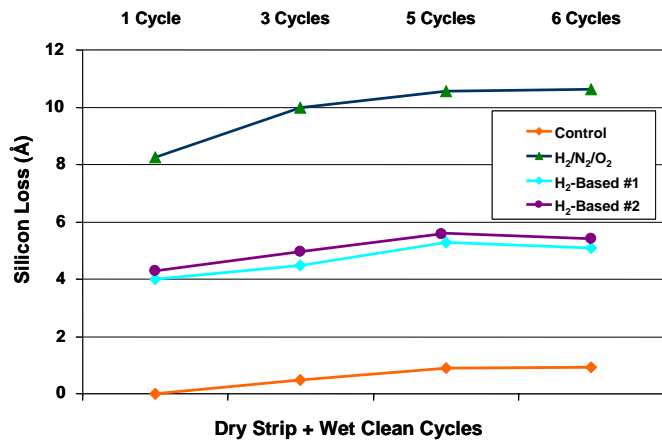
When we increase dry strip step time, as in the processes



with results shown in Figure 4, residues are more completely chemically broken down and can be removed by a DI rinse. In this case, the Si loss is as shown in Figure 6.

Figure 6. Cumulative Si loss for six cycles of combined stripping and DI rinse. Included are both reducing and oxidizing chemistries.

The total Si loss is growing very slowly, or not at all, for all process recipes at about five iterations of strip and clean. We expect, therefore, that total Si loss will remain at about 5 Å



through 10 or more high-dose implant steps, resulting in less than 0.5 Å of Si loss per step. There is, in fact, a negative SiO₂ loss since its thickness is greater following all strips and cleans than it was initially.

Having shown that Si loss is quite competitive for the new process chemistry, additional tests were done to demonstrate that this chemistry has no integration problems. One concern stemmed from absorption of atomic hydrogen observed in the implanted silicon. This might result in altered electrical or physical properties if the hydrogen remained in the silicon after anneal, or if it distorted the dopant profile in the silicon or de-activated it. Shown in Figure 7 are results of measurements of optical and electrical properties of non-patterned silicon wafers that were implanted (3 E15 doses for both As⁺ at 3keV and BF₂⁺ at 3 keV) and then exposed to strip processes. We found that sheet resistances for wafers exposed to reducing chemistry processes were less than, or

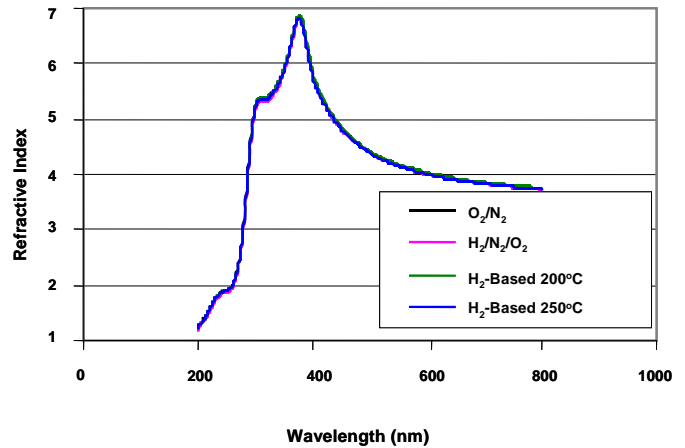
equal to, those for oxidizing processes for both As⁺ and BF₂⁺ species in all cases.

Figure 7(a)

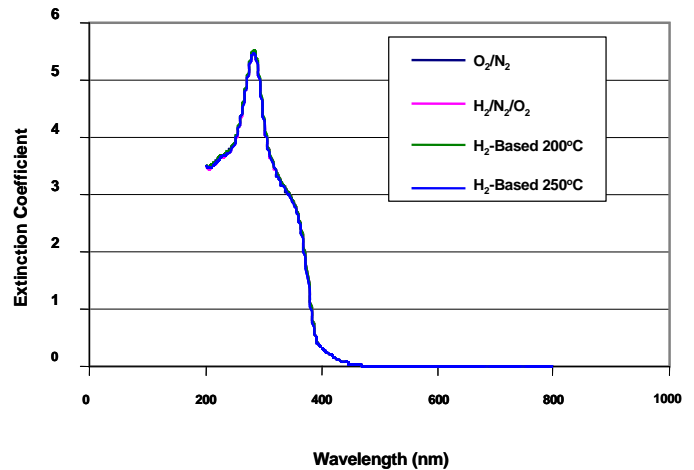
Refractive index for wafers doped with BF₂⁺ at 3 E15 and 3 keV after either reducing or oxidizing strip processes and standard 65 nm spike anneal.

Figure 7(b)

Extinction coefficient for wafers doped with BF₂⁺ at 3 E15 and 3 keV after either reducing or oxidizing strip processes and standard 65 nm spike anneal.



Refractive index and extinction coefficient of doped silicon measured after spike anneal are two sensitive indicators of its optical properties. Plots of these are shown in Figure 7(a) for refractive index and Figure 7(b) for extinction



coefficient with curves overlaid for wafers exposed to different strip process conditions. We observe very little difference between the tested strip conditions. When viewed at a highly magnified scale, the reducing chemistry curves in Figure 7 actually lie between those for the two cases of oxidizing strip chemistry. Similarly, optical scans for As⁺ implanted wafers show the same behavior, indicating no remnant effect after anneal of the hydrogen that might be absorbed into implanted silicon during stripping.

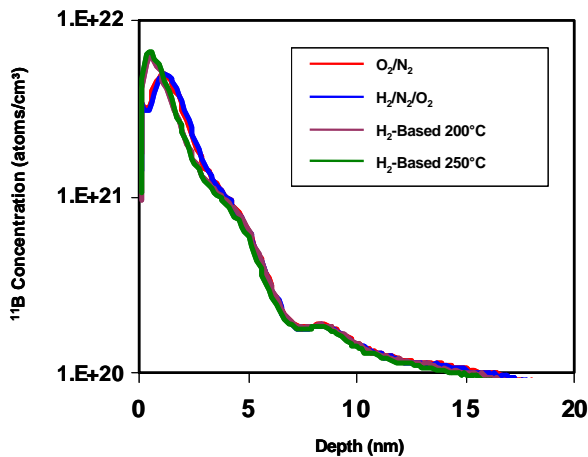
Finally, we did a surface SIMS measurement of the actual physical dopant depth distribution for both implanted species.

The results shown in Figure 8 demonstrate that the dopant is actually closer to the surface for the wafers stripped with H₂-Based gas chemistry relative to that for the Oxygen chemistry.

Figure 8

Depth distribution of boron for wafers following strip and spike anneal for different strip process chemistries in a reducing chemistry process.

The magnitude of the difference is substantial for the roughly 1.5 nm nearest the surface, where the concentration may be almost a factor of two higher for wafers that were stripped without use of oxygen. This may be desirable in minimizing



sheet resistance for the shallowest of junctions.[3]

Conclusions

Downstream stripping processes for heavily ion implanted (USJ) photoresist using hydrogen as principal reactant have been shown to result in more easily removed residues following dry strip, and less Si loss due to combined strip and clean than those stripped with gas mixtures containing oxygen. Further, wafers following hydrogen-based stripping processes, whether implanted with BF₂⁺ or As⁺ ions, under conditions such as those for USJs at the 45 nm node, show shallower dopant distributions, lower sheet resistances and identical Si optical properties when compared with wafers processed with conventional oxygen-based stripping chemistries. We conclude that hydrogen-based stripping processes should be seriously considered for next generation (45 nm node) device manufacturing.

Acknowledgments

The substantial efforts of Mr. Garry Montierth of PCT Systems of Fremont, CA. in all wet cleaning tests discussed in this paper are gratefully acknowledged. Further, many optical measurements of silicon properties, including those shown in this paper, were done with the gracious help of T. P. Sarathy of Nanometrics Corp. of Milpitas, CA.

References

- 1) "Process Technology for High-Dose Implanted Dry Strip at 65 nm and Beyond", Stu Rounds, Aseem Srivastava and Keping Han; Semiconductor Manufacturing, August 2006 p 28-32.
- 2) "45 nm-node USJs"; John Borland, Akira Mineji, Wade Krull, Masayasu Tanjyo, Robert Hillard and Tom Walker; Solid State Technology May 2006 Vol 49 pp 47-54.
- 3) "Low Temperature RTP for Source/Drain Engineering"; Juergen Niess, Wilfried Lerch, Silke Paul, Patrick. Schmid and Paul Timans. Solid State Technology June 2005, pp 37-42.